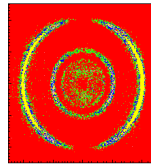


The **RoentDek** FEE front-end electronics for Delay-line readout



RoentDek

Handels GmbH

Supersonic Gas Jets
Detection Techniques
Data Acquisition Systems
Multifragment Imaging Systems

The read-out of delay-line and timing/counting anodes requires analogue electronics that shape the raw output signals so that the selected follow-up digital read-out electronics can effectively retrieve and store the time. Thus, TOF and position information coded in the individual signals' arriving sequence can be determined with high precision and throughput. Since the pulse heights of signals from MCP and delay-line (or timing) anode are rather small, adequate amplifying circuits are required before digitization and data acquisition. *Proper selection of bandwidth and impedance are crucial for optimal performance.* **RoentDek** offers several versions of amplifiers optimized for various read-out anodes. The basic version is the [FAMP1+](#), which is employed for the MCP timing channel of delay-line anodes and with [DET](#) detectors. Several other multi-channel versions exist (see [FAMP description](#)).

For detector read-out with fast ADC units (analog digitizers) such as the **RoentDek** fADC4 the FAMP modules already provide adequate signal shaping so that the timing information encoded in the signal sequence can be retrieved with great precision by the software after digitizing the analogue signal shape. Please refer to the [fADC4 description](#) for this advanced read-out method which is especially recommended for certain multi-hit read-out applications.

For standard detector read-out with TDC units (time digitizers, see [TDC description](#)) additional signal processing and discrimination circuits are needed. Since the width (rise time) of the detector signals (typically > 1 ns) is beyond the required timing precision so-called *Constant Fraction Discriminator* (CFD) circuits are necessary for further signal processing. Such circuits produce "digital" timing signals, e.g. NIM signals, from the amplified signals which represent the timing information on the signal with sub-ns precision which are suitable for digitization with TDCs and similar data acquisition modules. **RoentDek** provides several types of CFD units with up to eight channels (see [CFD description](#)) for operation in combination with adequate amplifiers.

Combinations between FAMP and CFD modules form the **RoentDek** FEE product family FEE2(x)/FEE5(x) for DLD and [FEE8/FEE7x](#) for delay-line detectors with [Hexanode](#).



Figure 1: FEE5x with 19" 3HU crate hosting six amplifier channels (FAM6L or two FAMP3) and 4+1 CFD channels (four CFD1c plus one CFD1x). The CFD1x has additional circuits to transform pulse height information into a time delay for recording by a TDC channel. **RoentDek** can also provide a CFD4c (NIM cassette) which replaces the four of CFD1c units on the right (no crates are provided if this combination is chosen). For cabling please refer to the [FEE5 connection scheme](#).

While the standard **FEE5** contains five **CFD1c** modules, the **x** version includes one **CFD1x** unit with additional circuits to transform pulse height information into a time delay for parallel recording on a TDC channel (see [CFDx description](#)).

For **Hexanode** read-out (or read-out of several **DLD** detectors) the **CFD8c/CFD7x** units (1HU, for 19" crates) are available. These are forming in combination with a **FAMP8** amplifier the [FEE8/FEE7x](#) product assemblies, respectively.

For **DLD** detectors **RoentDek** can provide alternatively the so-called **DLATR** circuits inside the **ATR19** units which contain both an amplifying stage and **CFD** stage for delay-anode read-out on a single board, two channels of each per board. The **FEE2(x)** product combination uses the latest version of the **ATR19-2b** two-channel model (see [ATR19-2 description](#)). One unit is required for read-out of one delay-line layer (i.e. two units are necessary for a **DLD**), in combination with **FAMP1+** and **CFD1c** (or **1x**) for reading out the MCP timing signal.

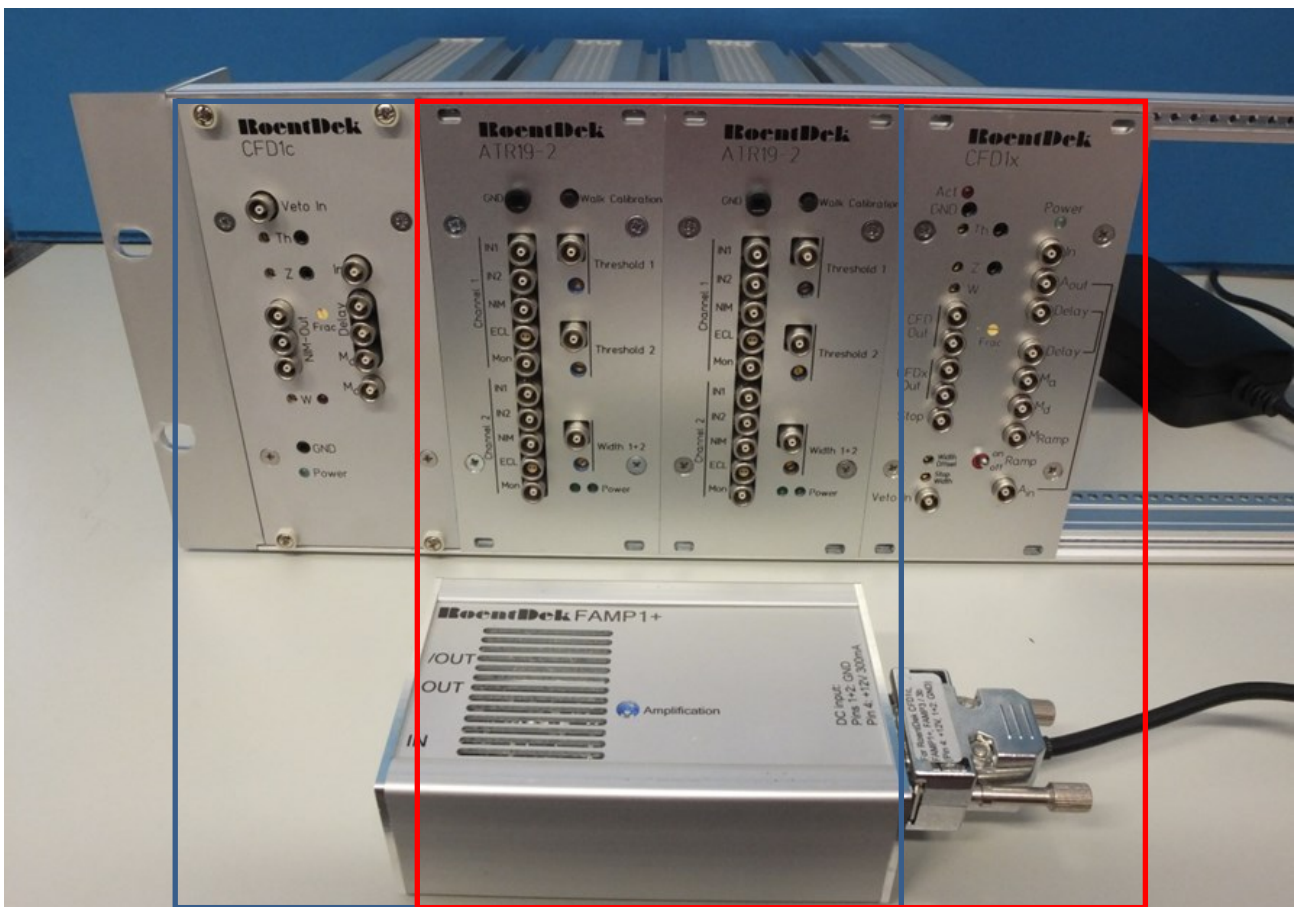


Figure 2: Examples of **FEE2(x)** product assemblies for **DLD**, mounted in a 19" 3HU frame (available on request). **FEE2**: Left three modules plus **FAMP1+** (blue rectangle). The **CFD1c** can be replaced by a **CFD1x** to form the **FEE2x**: right three modules with **FAMP1+** (red rectangle). Newer **FAMP1+** units have the gain potentiometer moved to front panel. The **FAMP1+** module is also available as 3HU unit for rack mounting. For cabling please refer to the [FEE2 connection scheme](#).

The **ATR19-2b** units are more compact and simpler to use and to adjust compared to the **FEE5** electronics. They should only be used with the standard helical-wire **DLDs** and give fewer options to address increased demands like optimal spatial resolution or lowest dead-time. They are not suitable for detectors with LC-delay-lines.